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Low power VVC decoding with OpenVVC - Extended Abstract*

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Recently, global demand for high-resolution videos and the new multimedia applications have created the need for a new video coding standard. Hence, in July 2020 the Versatil Video Coding (VVC) standard was released providing up to 40% bit-rate saving for the same video quality compared to its predecessor High Efficiency Video Coding (HEVC). However, this bit-rate saving comes at the cost of a high computational complexity, particularly for live applications and on resource-constraint embedded devices. This paper present a low power VVC decoder implementation designed for embedded platforms. This latter exploits three level of optimization to reduce the energy consumption for ARM architectures

The first level of optimization exploit the data-level parallelism inside different computation blocks. The source code of the *OpenVVC* decoder is heavily optimized with SIMD instructions. For ARM processor, NEON vector processing instruction set is well suited for performance optimizations. The most time consuming blocks including motion compensation, inverse transform, deblocking filter, Sample Adaptive Offset (SAO) filter Adaptive Loop Filter (ALF) have been optimized with NEON instructions.

The second level of optimization exploit high-level paralelism proposed by VVC through frame, tile and slice-based parallelisms. For frame-level parallelism, a main thread is used to parse the PSP, SPS, picture/slice header and schedule decoding threads with a thread pool. Then, the main thread provides the data and updates the internal structure of the available threads in the thread-pool for decoding the frame. Therefore, motion compensation synchronization between threads is performed for sequences with inter-coding configuration after starting the decoding process.

The third level of optimization exploit power management techniques. Data level parallelism and task level parallelism reduce the decoding time. This execution time reduction is translated into an energy consumption decrease thanks to Dynamic Voltage and Frequency Scaling (DVFS) which adapts the clock frequency and the voltage supply to the processing load. The challenge is to prediction the complexity of the forthcoming frame to decode.

The results showed that the OpenVVC decoder achieve real-time decoding of FHD resolution at 30 fps targeting a platform with 8 cores with a maximum frequency of 2.2 Ghz and HD

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real-time decoding at 30 fps for platforms using 4 cores with a maximum frequency of 1.8 Ghz. In terms of average consumed power, OpenVVC showed around 5.6 watts and 1.7 watts for the 8 and 4 cores platforms, respectively.

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