The Address-Event Representation Communcation Protocol

AER 0.02

February 17, 1993

1. Introduction

Many research groups are investigating communication protocols for electronic implementation of neural processing. One approach, the **address-event representation** (AER) [1,2,3,4], has attracted the interest of several research groups around the world. These groups intend to adopt this approach as the standard for their future projects, and plan to extend the concepts in [3,4] to solve related communications problems.

The purpose of this document is to establish a standard AER signalling protocol, so that implementations of AER from different research groups can communicate to each other. The document also provides guidelines for extending the standard; AER 0.02 specifies the minimal level of compatibility for AER.

This document does **not** specify hardware architectures or circuits for implementations. The document describes logical and electrical requirements for signals used in AER communication, but does not concern the structures that generate and interpet these signals. In addition, this document is not a tutorial or justification of the AER representation; see references [3,4] for this information. When this document is ready for distribution, it will be available electronically (pickup information goes here).

2. System Model

AER 0.02 only concerns the point-to-point, unidirectional communication of asynchronous data from an sender S to a receiver C, as shown in Figure 1. The connection between S and C consists of two types of wires, **control** wires and **data** wires.

The data wires are exclusively driven by S, and exclusively sensed by C. The coding of the data wires is not the subject of AER 0.02 ; the number of wires, the number of states on each wire, and the number representation of the data wires are all considered implementation dependent. Only the **validity** of the data wires are of interest in this document. If S is driving a stable signal on the data wires, suitable for robust sensing by C, the data lines are considered **valid**; if this condition does not exist, the data lines are considered **invalid**.

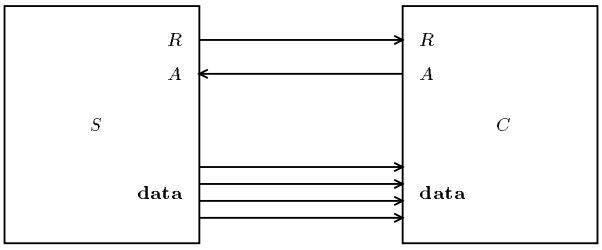

Figure 1. The system model, with sender S, receiver C, control signals request (R) and acknowledge (A), and implementation-dependent data wires.

In contrast, the timing and logical properties of the control wires are a major concern of AER 0.02 . AER 0.02 suggests, but does not require, electrical properties of the control wires.

3. Control Wires: Logic and Timing

AER 0.02 specifies the behavior of the control wires **request** (R) and **acknowledge** (A), and the validity of the data wires with respect to R and A. R is exclusively driven by S and is exclusively sensed by C; A is exclusively driven by C and exclusively sensed by S. Both R and A are binary signals, and can assume the asserted state **1** and the unasserted state 0. Section 4 will discuss the electrical properties of R and A.

Figure 2 shows the control sequence that communicates data from S to C. In the idle state, S drives R to logic 0, C drives A to logic 0, and the data lines are considered invalid. To begin a transaction, S first drives valid signals on the data wires, and then drives R to logic 1. In response, C senses this valid data; this sensing operation may take an arbitrarily long amount of time. Once C has sensed the data, it drives A to logic 1; by this action, C has removed the requirement of S to supply valid data.

Upon sensing A is at logic 1, S must drive R to a logic 0; S may take an arbitrary amount of time to perform this act. Upon sensing R is at logic 0, C must drive A to a logic 0; C may also take an arbitrary amount of time to perform this act. Once S has sensed A is at logic 0, it is free to start a new transaction. Only the logical transitions of A and R shown in Figure 2 are permitted to occur; for example, A is not permitted to transition from logic 0 to logic 1 if R is at logic 0.

The minimum timing requirements in AER 0.02 are specified with an empirical test. A sender compatible with AER 0.02 must supply a free-running stream of signals on the data wires, if the R and A control wires of the sender are connected together. In addition, the signals on the data wires must be valid whenever R is at logic level 1. A receiver compatible with AER 0.02 must sense a stream of valid addresses, if an inverted version of the A signal of the receiver is connected to the R of the receiver, and a valid address is present on the data wires. Future versions of the standard may augment this empirical test with more traditional specifications.

4. Control Wires: Electrical and Physical

We encourage AER 0.02 implementations with non-traditional electrical signalling methods. However, if an implementation uses voltages as the signal variable, AER 0.02 makes specific suggestions. AER 0.02 strongly suggests that, in the default mode of operation for an implementation, the logic 1 level for A and R is more positive than the logic 0 level for A and R. In addition, AER 0.02 strongly suggests implementations support multiple modes of signal polarity; ideally, the electrical polarity of A and R can be changed, either by physical contact (reconfiguring signals or straps) or under programmed control.

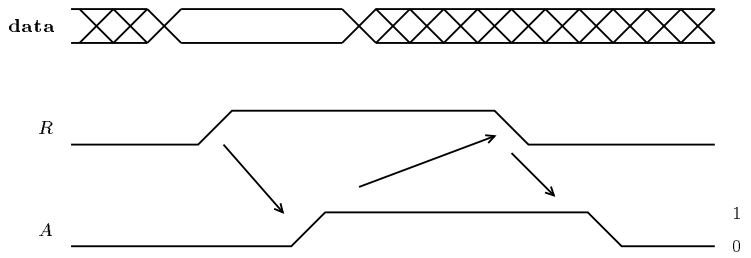

Figure 2. Logic diagram for a communications sequence, with control signals A and R, and data lines (crosses indicates invalidity).

5. Compatibility Requirements

AER 0.02 is a minimal communications standard, and it is expected that research groups will augment the standard to add new functionality. Indeed, future versions of the standard will largely be the codification of enhancements that have been successfully implemented. This section proscribes guidelines for extensions of AER 0.02 .

In an extended AER 0.02 implementation, it must be possible to non-destructively disable all extensions. This disabling may require physical contact (reconfiguring switches or straps), or may be performed by changing state inside the implementation through external programmed control. In this "backward-compatibility" mode, the implementation must supply A and R control signals and data wires that perform as required by AER 0.02 .

6. References

[1] M. Mahowald, Ph.D. Thesis, Computation and Neural Systems, California Institute of Technology, 1992.

[2] M. Sivilotti, "Wiring Considerations in Analog VLSI Systems, with Applications to Field-Programmable Networks," Computer Science Technical Report (Ph. D. Thesis), California Institute of Technology, 1991.

[3]Lazzaro, J., Wawrzynek, J., Mahowald, M., Sivilotti, M., and Gillespie, D. (1993). "Silicon auditory processors as computer peripherals," *IEEE Transactions of Neural Networks,* May (in press).

[4]Lazzaro, J., Wawrzynek, J., Mahowald, M., Sivilotti, M., and Gillespie, D. (1993). "Silicon auditory processors as computer peripherals," In Moody, Hanson, Lippmann (eds) *Advances in Neural Information Processing Systems 5.* San Mateo, CA: Morgan Kaufmann Publishers.