Prototyping the Li-Fi System Based on IEEE 802.15.7 PHY.II.1 Standard Compliance

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Abstract—By using Visible Light Communication (VLC), in contrast to radio waves, the secure connection can be established more efficiently since the visible light could not radiate through most solid objects. VLC has been applied for many use cases, one of them is Light-Fidelity (Li-Fi). With Li-Fi, internet access is no longer using conventional RF spectrum as employed in Wi-Fi technology but apply visible light. In this paper, we present the design and implementation of a Li-Fi on a System on Chip (SoC) with a low-cost discrete analog front end (AFE). We used ZYBO Zynq-7000 as a digital signal processing, 8 Watt yellow-colored high-brightness LED (HBLED) for downlink transmitter, and 3 Watts infrared LED (IR LED) for uplink transmitter. Our system is developed compliant with the IEEE 802.15.7 standard, i.e. PHY II.1. According to the result, our Li-Fi system makes the PC/Laptop connected to any internet sources with a maximum speed up to 500 kb/s, and the maximum optical channel distance (range between the light source and the light receptors) is about 110 cm with two lenses.

Index Terms—IEEE 802.15.7, Li-Fi, system-on-chip, visible light communication

I. Introduction

Visible Light Communication (VLC) is an emerging technology with rapid development nowadays. VLC is considered as a compliment and successor of Radio-Frequency (RF) communication, and it has several advantages over RF. The first advantage of VLC is the utilization of the electromagnetic wavelength (430 to 770 THz) which is a free slot spectrum because it has not been utilized as a medium for the data transfer (free license) [1]-[3]. Second, by using VLC, the LED that is generally used only for lighting purpose can be simultaneously employed to connect one or more personal computers to the internet source. Third, VLC utilizes the physical properties of light waves that are unable to penetrate most of the solid material. Hence the connection can be maintained in a single room alone. It can optimize the user's convenience and security aspects of the created network. Also, VLC technology capable of being used in closed locations where it may be impossible to use the RF links, e.g. in a hospital, free-electromagnetic area, or an aircraft cabin.

IEEE 802.15.7 is a standard for VLC implementation that defines two layers, i.e., the MAC layer and PHY layer [4]. The PHY layer must implement one of three operating modes available, namely I, II, or III [5], this standard operating mode uses channel coding services for error correction. The PHY I use concatenated coding with Reed-Solomon (RS) and convolutional coding (CC) because this standard is designed for use in outdoor areas with short frames. While PHY II and PHY III only use RS coding. Like PHY II, the PHY I also use Run Length Limited (RLL) code to provide DC balance, clock recovery, and flicker mitigation. Aside from the type of modulation and coding, various optical rates are also provided for each type of PHY to provide support for different LED specifications in a variety of applications.

Some prior works have observed, explored, and implemented IEEE 802.15.7 standard, such as [6]-[9]. *F. Che et al.* designed and implemented PHY I transceiver, they succeeded to obtain data rates from 11.67 to 266.6 kb/s and bit error rate (BER) of 10^{-6} when the received illuminance is 18 Lux [6]. Similar to [6], *P. Namonta et al.* also used PHY-I for real-time vital sign transmission, they shown successful transmission of temperature and heart rate in 100 kb/s with a maximum of 590 cm [7]. Later, *A. Musa et al.* reported the VLC development followed IEEE 802.15.7 standard for real-time video transmission [8]. **But** they do not specify the PHY used in their system. Later, *E.S. Rahayu et al.* explored IEEE 802.157 PHY I, but they do not implement to the real system since their study only in the simulation phase using Matlab [9]. Related to VLC realization with standard compliance, there are fewer works that tackle TCP/IP transmission over visible light utilizing SoC-based FPGA. *A. Sturniolo et al.* have integrated the common commercial lamp successfully with Ethernet 10Base-T transmission over a NDLOS link with 12.5 Mbit/s transmission of a Manchester coded on-off keying (OOK) signal. SoC-based FPGA was used, and they claimed that the designed VLC system could be used over a distance of 1 meter in NDLOS and BER of 10^{-9} [10]. **However**, in [10] is not informed whether the Ethernet-enabled VLC implementation follows the IEEE standard or not.

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In previous work, we reported bidirectional VLC implementation for internet access (Li-Fi) based on IEEE 802.15.7 standard [11]-[13]. In [11], we discussed the rapid SoC design. In [12], we presented the MAC layer implementation (point-to-point), while in [13] we reported Li-Fi system performance. Our system can perform in exchanging TPC/IP data. Therefore, it can connect to the internet, and it has been demonstrated successfully in ping-test and browsing. **Nevertheless**, we got only 11 kb/s that is very slow and do not apply PHY layer to the Li-Fi system, yet. A much higher internet connection speed is needed so that users can use various existing internet services (either browsing or streaming) comfortably.

The motivation of this research is to improve the Li-Fi system performances as reported in [11]-[13], which includes: 1) speed of internet access, i.e., from 11 kbps to 500 kbps; 2) the optical distance of the connection ranges from 3 cm to 1 m, 3) replace the Analog Front-End (AFE) receiver so that it can be clocked up to ~ 1 MHz because previously only 100 KHz. In this paper, we implement a PHY layer consisting of the forward error correction (FEC) and modulator/demodulator using the hardware description language that complies with the IEEE 802.15.7 standard, which in [11]-[13] is still implemented with USART communication. To reach 500 kb/s, we used PHY II option instead of PHY I. Hence, the variable pulse-position modulation (VPPM) modulation is used, and it will be implemented in the SoC-based FPGAs, that is Zynq 7000 processor (ZYBO board). Moreover, we compare this system specification to the IEEE 802.15.7 PHY II.1 standard.

This paper is organized as follows: 1) introduction discusses the research motivation, 2) system design presents the system block diagram of Li-Fi, processor used, PHY, datalink, network, modulation used, and analog-front end transmitter-receiver (transceiver) design using LED switch topology, 3) results and analysis, and the last is 4) conclusion and addressing the future work.

II. System Design

A. System Block Diagram

Fig. 1 shows the block diagram of the proposed system; it comprises two subsystems, i.e. the baseband processor part (for host and client) and the AFE transceiver part. The host-side of LiFi system is connected to internet source to provide internet connectivity, which can be any OSI layer three devices, using an Ethernet cable or USB cable whichever preferred. The user will interact using their personal computer (PC) as he/she would normally do while accessing the internet. The user's PC is then connected to the client-side through an Ethernet cable. Either side of the AFE is connected through a wireless channel by using white HBLED-Photodiode pair for downlink connection, and by using IR-Photodiode pair for uplink connection.

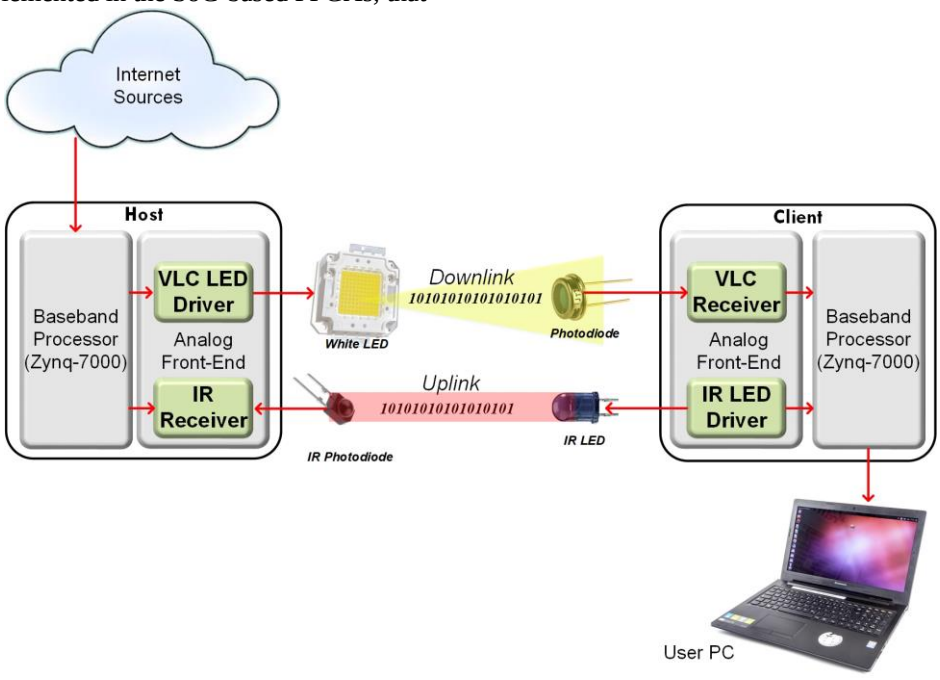

Fig. 1. Proposed system block diagram.

In our system, the baseband processors are implemented on an All Programmable System on Chip (APSoC), we employed Zynq-7000 which is hosted on a development board from Xilinx, ZYBO. Whereas the AFE transceiver is built by using discrete components and printed in through-hole PCB.

To design the Li-Fi, we followed IEEE 802.15.7 standard, that is PHY II.1. The standard chosen by Li-Fi that will be made in this work is for high data-rate in indoor environment applications. The PHY II.1 specifies the clock rate about 3.75 MHz, but we set at 2 MHz to match the AFE capabilities made. Moreover, we used

VPPM modulation with RLL coding 4B6B, FEC (64,32) and RS coding as defined in [5].

B. Processor

To select an FPGA development board for Li-Fi prototyping, we consider four factors, i.e. availability in the market, prices, features, and performances as suggested by [14]. Table I is a comparison of several alternative options for FPGA development boards, namely ZYBO, MicroZed, and ZedBoard.

TABLE I: FPGA BOARD COMPARISON

Capabilities	ZYBO	MicroZed	ZedBoard
Cost	189 USD	199 USD	395 USD
Chip SoC	ZC7Z010-1CLG400C	XC7Z010-1CLG400C	XC7Z020-CLG484-1
SD Card	MicroSD slot	4 GB MicroSD card	4 GB SD Card
GPIO Connector	Pmod Connectors x 6	2×6 Pmod exposes 8 PS MIO	Five 2×6 Pmod headers exposing 32 PL I/O and 8 PS MIO
Ethernet	1G/100M/10 Mbit Ethernet	10/100/1000 Ethernet	10/100/1000 Ethernet
ADC	No analog	No Analog	XADC header
RAM	512MB x32 DDR3	1 GB of DDR3 SDRAM	512 MB DDR3

Concerning the price factor, the ZYBO board is the most excellent because it is the cheapest. While concerning the SoC chip, the entire chip meets the considerations, because all three boards have ARM and FPGA processor parts that are connected by a bus. All three boards have an SD card and it have GPIO connectors because only two pins are needed (one for transmitting and one for receive). Later, in respect of Ethernet connections, all boards have the same speed. While concerning analog signal processing, just the ZedBoard board has. However, because of the signal sent to the analog part is only needed for switching, the absence of an ADC is not problematic. About the RAM size, all three are enough to run Linux OS. In summary, with regard to the considerations, we select the ZYBO due to meet all quality requirements and sell at a relatively lower price compared to the other two boards.

Fig. 2 depicts the baseband processor architecture implemented on APSoC Zynq-7000 chip. The system can be separated into two parts: the ARM processor core which runs Xillinux OS and the programmable logic. The PHY of the communication system is implemented as several separated IPs on the programmable logic fabric while the data link and network layer are implemented in a multithreaded program, which is run on the ARM processor core fabric through Xillinux. Furthermore, there are also PHY and MAC chip, which is included in the ZYBO board, to connect the APSoC with a PC or the internet source.

The programmable logic side interacts to the ARM processor core side, vice versa, trough AXI bus, and DMA buffers. However, both the program or any of the IPs interacts directly with the AXI bus nor the DMA buffers. Instead, they interact through an additional interface. On the programmable logic side, that interface is a series of FIFO buffers and a Xillybus IP. While on the ARM processor core side, that interface is device files and drivers accessed by the program through read/write operations. Both the Xillybus IP and device files and drivers are customized for this specific application and can be requested trough Xillybus Ltd. website.

The ARM processor will run a program with five threads, i.e. *SendlightHandler*, *ReceiveLightHandler*, *SendEthernetHandler*, *ReceiveEthernetHandler*, and *SendACKHandler* that presented in a different report [15]. The developed baseband processor will handle 3 layers from OSI 7-layers model, i.e. PHY, Data Link, and Network which is described in the Section II.C.

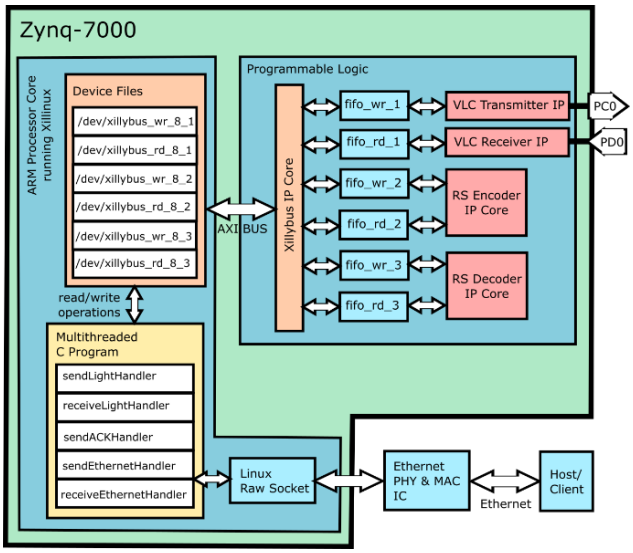

Fig. 2. Baseband processor architecture

C. PHY, Data Link, and Network

Fig. 3 illustrates the frame structure of the PLCP Service Data Unit (PPDU) that specifies in 802.15.7 PHY layers. Preamble field is used by transceiver to obtain the optical clock synchronization with packet that will enter. The first pattern sent is fast locking pattern (FLP). While the second pattern sent is topology dependent pattern (TDP) as illustrates in Fig. 4. The preamble part is transmitted using the OOK modulation type. PHY header is filled with information(s) that are useful for the receiving side. Table I is the content of the PHY header that comprises: Preamble, PHY Header, and PSDU slot. The header check sequence (HCS) section (a CRC-16 from the header) is useful for protecting PHY headers from undetected errors.

While a stop-and-wait automatic repeat request (ARQ) algorithm is implemented on the data link layer to prevent congestion on the transport layer while what happens is there are packet losses on the data link layer.

In addition, network address translation is implemented on the network layer to provide routing capabilities. The NAT, ICMP, UDP, TCP, and IPv4

protocols are supported in our system to enable the use of common internet services.

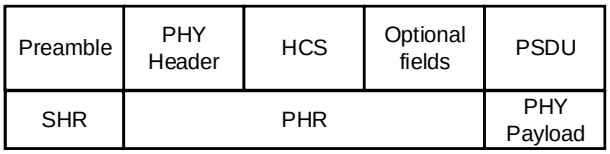

Fig. 3. Structure of PPDU frame [5]

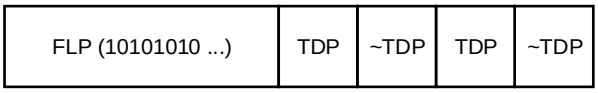

Fig. 4. Illustration of preamble field contents [5]

TABLE II: PHY HEADER CONTENT

Capabilities	ZYBO	MicroZed
Burst mode	1	Reduce preamble and IFS
Channel number	3	Band plan ID
MCS ID	6	Provide information about PHY type and data rate
PSDU length	16	Length up to a Max PHY Frame Size
Dimmed OOK extension	1	Information on compensation time, resync, and length of sub frame
PHY header fields	**Bit-width**	**Explanation on usage**
Reserved field	5	Future use

The IEEE 802.15.7 standard also provides a specification for the frame structure to be used in this work as shown in Fig. 5.

Number of bits	**64-bits upto 16.385 bits**	**60-bits**	**48-bits**	**24-bits**	**Arbitrary**
Function	*FLP*	*TDP*	PHY Header	*HCS*	*PSDU*
Modulation Scheme	*OOK*	*OOK*	*OOK*	*OOK*	*VPPM*

Fig. 5. Frame structure as specified on IEEE 802.15.7 [5]

D. Modulation

There are two types of modulation used in the IEEE 802.15.7 PHY I and PHY II standard: OOK and VPPM modulation. Both types of modulation can be classified as digital modulation where the number of possible symbols sent is limited. In the case of these modulations, there are only two symbols that can be transmitted, namely symbols that represent as "1" and "0". These two symbols are different from the two types of modulation discussed in this section.

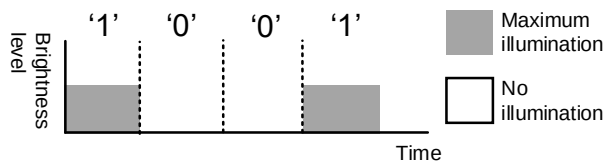

Fig. 6. Illustration of OOK modulation

Because this communication system uses visible light signals, the shape of the signal will correlate directly with the illumination level. For this reason, a high signal will be interpreted as maximum luminance of the LED transmitter, while a low signal will be interpreted as no illumination at all.

The OOK represents symbol "1" (a high signal) that continues throughout the symbol period while the symbol "0" is represented by a low signal that lasts continuously in the symbol period. Fig. 5 depicts the illustration of OOK. While the VPPM modulation represents symbol "1" (a high signal) that lasts for a fraction of the symbol period, then followed by a low signal that lasts for the remainder of the symbol period. Whereas symbol "0" is represented by a low signal that lasts for a fraction of the symbol period, then followed by a high signal that lasts for the remaining time of the symbol period.

The value of the high signal fraction in one period of symbol "1" or the low signal fraction value in one period of symbol "0" can be set according to the desired level of illumination during the data transmission period. For example, if the desired level of illumination is 25% and the period value of the selected symbol is 1 μs, then the period of high signal in one period symbol "1" is 250 ns (signal low for 750 ns after) while the period of low signal in one period symbol "0" is 750 ns (signal high for 250 ns afterward). Fig. 6 is an illustration of VPPM modulation for three different lighting values.

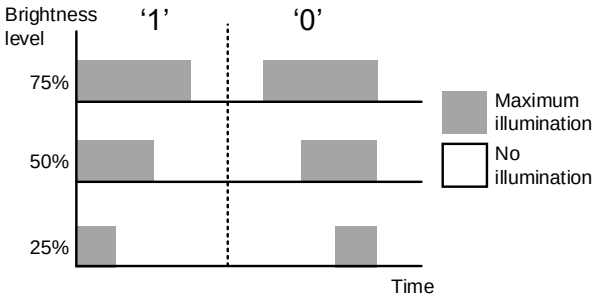

Fig. 7. Illustration of VPPM modulation

E. AFE Transceiver Design

Fig. 7 shows the schematic of the AFE receiver that can be divided into 5 sub-systems, namely, a photodiode module, a buffer, a passive HPF, a comparator, and a Schmitt trigger.

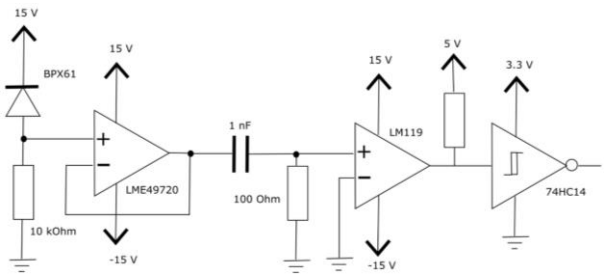

Fig. 8. AFE receiver schematic

A photodiode module has a function to capture the optical signal transmitted by HBLED and send the same signal to the AFE receiver. In this work, we used a voltage divider configuration for a photodiode module

rather than the TIA circuit usage [16]. A BPX61 photodiode provided by OSRAM was chosen because it has a sensitivity range of 400-1100 nm where the yellow light (570-590 nm) can be appropriately detected. Also, the BPX61 photodiode has a good lighting sensitivity level at 1000 lx. The higher light level (intensity) of LED, the higher output voltage of the photodiode module, as evidenced by [17].

The buffer stage is used to isolate the previous stage from the next stage. We used LME49720 as buffer's Op-Amp. It has GBW of 55 MHz. The next stage is the RC passive filter. While in comparator stage, we used LM119 that converts analog signals received into digital signals. However, the square wave edges are not sharp enough. Therefore, a 74HC14 Schmitt trigger is involved in the last stage of the AFE receiver.

The LED Driver Module is a circuit with a function to forward the light-modulated signal on the host-side into the photodiode module. The specification of the LED Driver used is a 3.3 V digital input signal for high-value data signals and 0 V for low-value. The power supply voltage applied is 15 V. We employed multichip Cree LED Array with yellow light. It requires a forward voltage (V_f) of 12 V with the forward current (I_f) ranging from 350 mA-1500 mA.

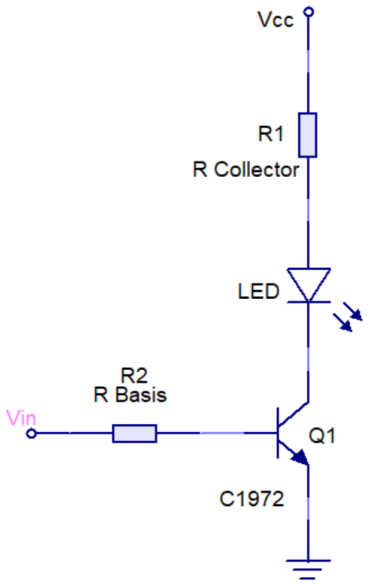

Fig. 9. Switch LED Driver for downlink

To perform the LED driver function as aforementioned, we selected the switch driver topology as in [18] in which the LED Driver circuit uses a common emitter configuration (Fig. 9). We utilized Transistor BJT type, C1972 model, from Mitsubishi Semiconductors. It can perform at high frequencies up to 175 MHz. Moreover, it can control the collector bias current (I_c) up to 3.5 A. The BJT C1972 has a specification as follows: V_{CE} (sat) = 0.2 V; V_{BE} = 0.7 V; and *hfe* = 50. Based on the Dataset, the value of R_C, R_B, and I_B can be calculated by using Eq. (1) to Eq. (3), respectively. Therefore, we obtain R_C = 2.8 Ω, I_B = 20 mA (using I_c = 1 A), and R_B = 130 Ω.

While the IR transceiver design for uplink connection, we utilized circuits similar to Fig. 9 and Fig. 10 but the difference is the optical component used: LED (3W IR LED) and photodiode receiver (KODENSHI SP8-ML).

$$R_C = \frac{V_{cc} - V_f - V_{CE(sat)}}{I_f} \quad (1)$$

$$I_B = \frac{I_c}{h_{fe}} \quad (2)$$

$$R_B = \frac{V_{in} - V_{BE}}{I_B} \quad (3)$$

III. Results and Analysis

A. Li-Fi Hardware

The hardware implementation of IEEE 802.15.7 PHY.II.1 Li-Fi system is visualized in Fig. 10. It consists of ZYBO FPGA development boards (host and client), power converter, AFE transmitter and AFE receiver modules for downlink-uplink connection, CREE HBLED as VLC antenna and photodiode module. Since this research still in the proof-of-concept phase, we have not packed following the consumer-based standard.

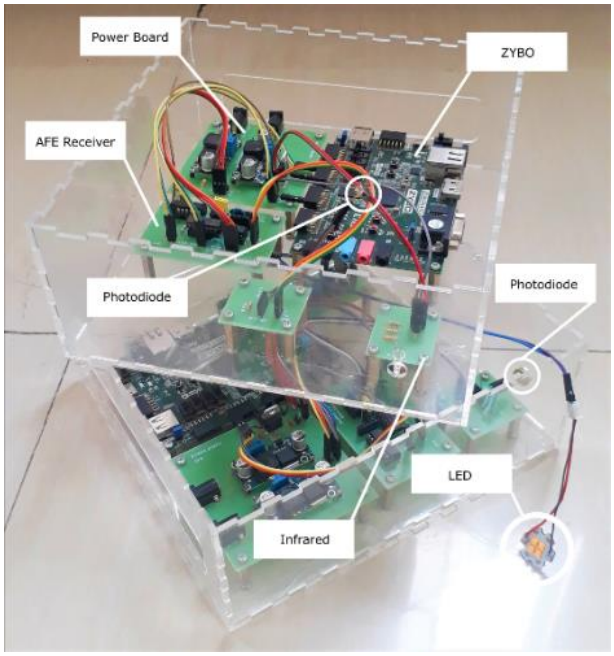

Fig. 10. Li-Fi module contains DSP boards and AFE transceiver

B. Observing the Transmission Format

Observation of the VLC transmission format aims to determine whether the form designed is following the IEEE 802.15.7 standard or not. The testing scheme is as follows: 1) connecting the Li-Fi client output with the logic analyzer, 2) running the data transmission and 3) observing the format. The IEEE 802.15.7 standard was used with reducing some parts that are not needed; it aims to reduce the data redundancy. The visibility pattern is not involved because it is not classified as data but only to maintain consistent visibility as long as the data is not

sent. Fig. 11 shows the VLC data transmission format using the logic analyzer. It can be concluded that the package frame structure has been implemented in the DSP. The package frame structure obtained is shown in Fig. 12.

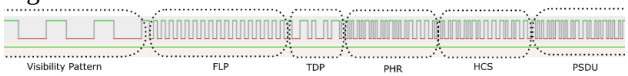

Fig. 11. Waveform obtained from the testing

Compared to the PHY specifications on the IEEE 802.15.7 standard (Fig. 5), there are two differences as follow:

1) The number of FLP and TDP bits, where the number of selected bits is less than specified as in the standard. The redundancy can be minimized but still enough to be easily implemented in the RTL design (multiples of 12-bit)
2) Modulation scheme of PHY header and HCS, the VPPM modulation scheme was chosen so that the RTL design can be much simpler. In addition to the preamble parts (FLP and TDP), the detection can use the same detector until the end of the transmission, namely the VPPM modulation detector.

Number of bits	**36-bits**	**12-bits**	**24-bits**	**24-bits**	**Arbitrary**
Function	*FLP*	*TDP*	PHY Header	*HCS*	*PSDU*
Modulation Scheme	*OOK*	*OOK*	*OOK*	*OOK*	*VPPM*

Fig. 12. Frame structure implemented

C. Encoding and Decoding Function

This test shows that RS encoder and RS decoder are very necessary for the Li-Fi systems, even for the condition of no error at all. With RS encoder/decoder, a BER value less than 10^{-3} can be achieved. But, if the channel has produced many errors, the RS encoder/decoder will not be able to correct it anymore as it can be seen in Fig. 13.

When the p_{11} value is higher than 0.4, BER value with encoding or without encoding is the same.

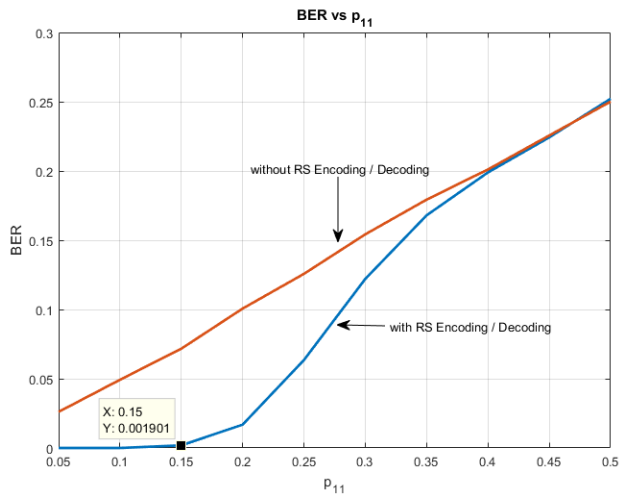

Fig. 13. The role of RS encoding/decoding for the Li-Fi system

D. Link Speed Test

Fig. 14 shows the comparison of bitrates in different operating conditions. The results obtained in real test is pointed in the blue-colored graph while the yellow graph shows the maximum achieved link speed theoretically if there is no redundancy at all. In the laboratory test, there is limited speed of the designed program to receive packets and there is no lag between packets that arrive.

As depicted in Fig. 14, it appears that all the link speed values obtained are lower than the theoretical value. This happens because of the redundancy factor: the limited speed of the program in "receiving" and then processing a packet before it can receive and process the next packet. Also, it is due to a delay between "sending" packets to send a data packet.

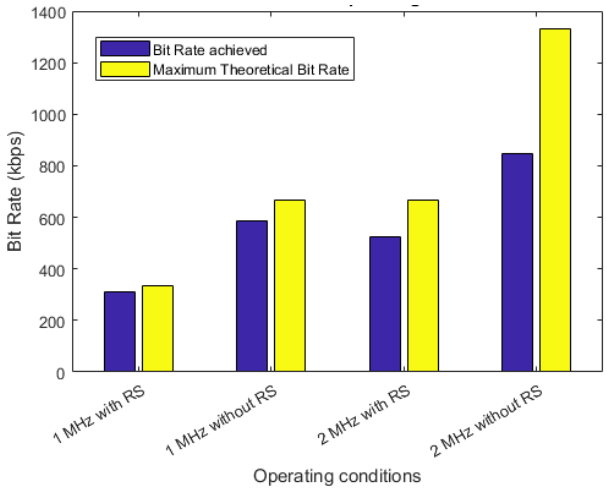

Fig. 14. The role of RS encoding/decoding for the Li-Fi system

The higher the theoretical speed, the further the obtained speed value. In other words, redundancy becomes more significant at higher rates. It is because of increasing the transmission speed linearly, does not affect the program to run more linearly, but the program runs at a constant speed.

E. Functional Test

We first measure the HBLED light intensity with 15 V supply and obtain 14040 lx; this value is sufficient enough to be processed by photodiode because the minimum sensitivity level of BPX61 photodiode is about 1000 lx. Fig. 15 visualizes a photograph of the demonstration. Two lenses are involved, it was installed between the light source and the receiver to increase reception range up to 110 cm.

The internet source used for all of demonstration and testing purposes is a USB-tethered smartphone, connected to the host-side trough a USB cable. Firstly, we set smartphone in tethering mode. Later, we tested Li-Fi system capabilities in handling internet protocol requests by using three common internet services, namely: pinging, browsing, and audio-visual streaming.

In summary, the Ping test was successfully demonstrated; it can be run from a Linux terminal and Windows command prompt. Then, the Browsing test was

performed by Google Search and also by opening several sites from search queries. To perform audio-visual streaming, our Li-Fi system was tested to stream the 360p quality video with minimal buffering required in Youtube.

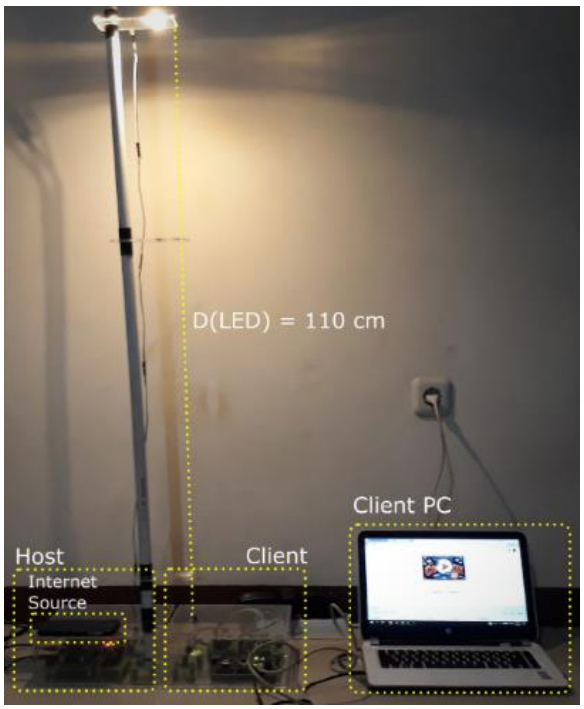

Fig. 15. A photograph of experimental setup

F. Internet Connection Speed

Additionally, we measure the internet connection speed through a website *testmy.net*. We obtain that the maximum speed of our Li-Fi system is 550 kb/s in which it is not much different from the maximum theoretical speed of 666 kb/s. We measure the connection speed data as shown in Fig. 16. The network speed test in downloading 500 kB of random data. The average connection speed is about 300 kb/s.

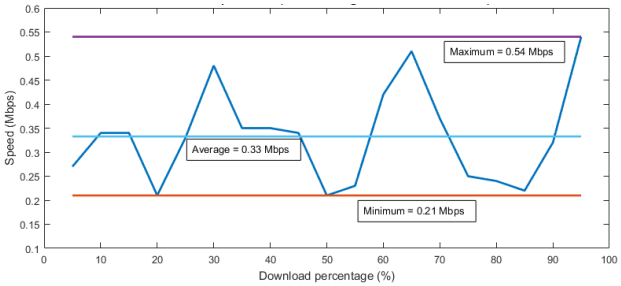

Fig. 16. Internet connection speed measurement (download connection). The speed instability is a natural thing in internet connectivity which may be caused by several factors, e.g., the result of a pause effect in running threads sent by Ethernet packets, the OS performs other processes, the TCP congestion control, or other external factors.

G. BER Evaluation

Lastly, we tested out the bit error rate (BER) performance for several distances of HBLED to Photodiode with two gain adjustment options in the AFE receiver, suppose Gain = 1 and Gain = 2. In this test, the lenses are not used to simplify test settings. The results of BER measurement are then plotted in Matlab as shown in Fig. 17. It can be concluded that zero BER is obtained until the HBLED-Photodiode distance is 5 cm if RS forward error correction is used. Moreover, we have observed that increasing the receiver's gain may increase the reception range, but it does not improve the BER performance. Thus, the best solution is to still involve the two lenses as depicted in Fig. 15.

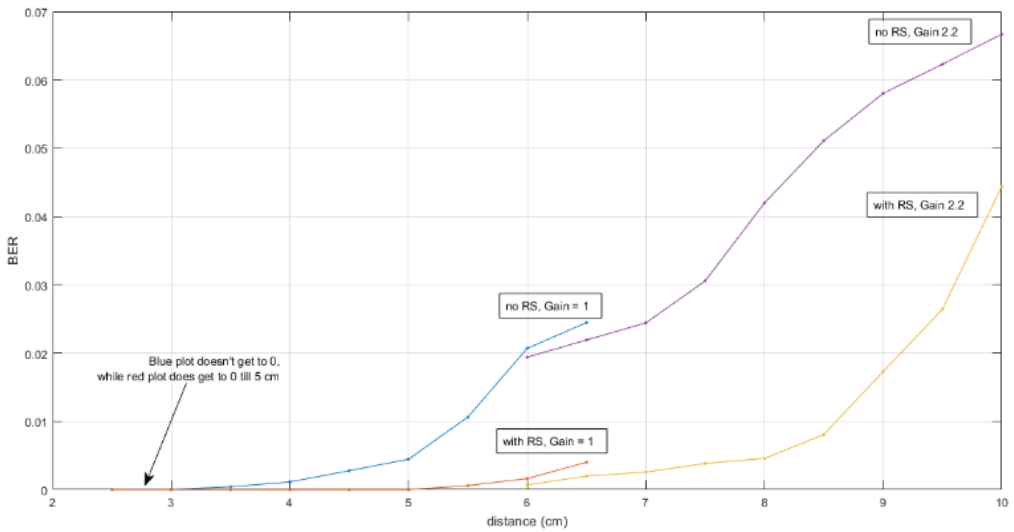

Fig. 17. BER performance measurement against optical distance

IV. Conclusion and Future Works

The Li-Fi prototype for internet access is presented in this paper. We used the IEEE 802.15.7 standard as guide for implementing the VLC PHY layer, that is PHY II.1. According to the functional tests, our Li-Fi system can perform well as expected, i.e. Pinging, Browsing with a connection speed of ~300 kb/s, and Streaming Youtube. BER measurement were also carried out in this research.

Since our Li-Fi system was utilized two lenses, so it requires direct LoS link meaning that the Li-Fi receiver should be set stationary (not moveable device). Although applying IEEE 802.15.7 standard, our system differs a little bit from the specification given as summarized in Table III. The difference in data transfer speeds is reasonable when using off-the-self components, due to several factors, i.e., optical noises, electronic noises, analog limitations related to bandwidth, DSP limitation (jitter), etc. In conclusion, our Li-Fi system has a better performance compared to previous work, as in [11]-[13].

TABLE III: IEEE 802.15.7 PHY II.1 STANDARD COMPARED TO THE IMPLEMENTED SPECIFICATION

Parameters	IEEE 802.15.7 PHY.II.1	Our Li-Fi system
Modulation	VPPM	VPPM
FEC	RS (64,32)	RS (64,32)
RLL	4B6B	4B6B
Optical clock	3.75 MHz	2 MHz
Achievable data rate	1.25 Mb/s	666 kb/s

To upgrade the Li-Fi system bitrates similar to the optimum data rates as defined in the IEEE 802.15.7 PHY.II.1 standard, the Li-Fi system packaging must be considered. In this work, we use a lot of wire (jumper) in connecting AFE block to DSP block. With a compact package, electronic noises can be minimized resulting in higher throughput and lower latency. Another option is to replace the VPPM modulation to OFDM technique as proposed by [19] to obtain more extensive bandwidth in the optical wireless system, and also implemented on a chip as suggested by [20].

CONFLICT OF INTEREST

The authors declare no conflict of interest

AUTHOR CONTRIBUTIONS

S.F., F.I., E.S., and T.A. proposed the concept; S.F. designed the analog circuit; F.I. and E.S. designed the system-on-chip architecture, lay-outed and printed the PCB. F.I. and S.F. carried out the experimental data. F.I. analyzed the data; S.F. contributed to writing of the manuscript and drawn illustrations; E.S. contributed to proof-reading the paper. T.A. supervised the research; all authors had approved the final version.

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