REAL TIME SAR PROCESSING TECHNIQUES

by Roland Schotter

DORNIER SYSTEM GmbH
P.O.B. 1360
D-7990 Friedrichshafen
Federal Republic of Germany

Abstract

Spaceborne Synthetic Aperture Radar systems provide raw radar data information at high data rates of 10 Mwords per second. Real time SAR processors, therefore, must perform more than 1 giga-operations (multiplications, additions) per second in order to generate images from the raw data. Since conventional computer systems are not able to cope with these requirements DORNIER has developed real time SAR processors on the basis of a modular pipeline concept.

The processing pipeline is built up of standardized hardware modules which are required for digital signal processing of two-dimensional data. These modules show identical electrical and mechanical interfaces so that each hardware module can be used in any place of the pipeline.

The paper presents the basic principles of the real time modular pipeline concept and its processing rate requirements for real time SAR processing applications. The implementation of some of the most important modules like Fast Fourier Transformation, correlation, interpolation and data memory is described.

Finally, a short outlook on further applications of the pipeline processing concept is given.

Introduction

Synthetic Aperture Radar images (SAR images) of the earth are an important tool for many scientific ranges and application related problems. Due to the fact that radar waves are able to penetrate even through strong clouds at very low attenuation, SAR images are available day and night independent of weather conditions.

SAR data can be applied in a multiple way. In oceanography theories on the origin and extension of ocean waves can be investigated. Limits between iced and iceless areas can be detected by means of SAR images as well. This facilitates for example finding optimum ship navigation courses and the operation of ocean platforms in polar areas. Since icebergs are detectable in SAR images, SAR information is also predestinated to be applied in iceberg warning.

The scattering coefficient for radar waves mainly depends on the water content of the illuminated objects. Therefore, conclusions on the growth conditions of vast agricultural areas can be derived from the radar images (wheat and tobacco fields, detection of forest damages). Geological structures are often clearly visible in SAR images so that radar images can be used in this field, too. This applies mainly for the exploration of hardly accessible areas.

Further applications can be found in overall ship control (200 miles zones, environmental oil pollution monitoring on sea), in archeology and glacier research.

Most of the above mentioned applications require real-time conversion of SAR raw radar data into images for its efficient use. For this reason DORNIER has implemented a digital real-time SAR processor for earth exploration in the framework of a BMFT/ DFVLR contract. The missions ERS 1 (C-band) and X-SAR (X-band) are intended to be the first applications of the developed SAR-processor.

The SAR System

The complete SAR system consists of a sidelooking radar and a SAR processor which converts raw radar data into SAR images. The basic geometry of the SAR is shown in Fig.1. The radar antenna travelling at uniform speed illuminates a certain swath on ground which returns radar echos to the antenna according to its reflectivity. These signals are converted in several steps from the carrier frequency band into the baseband by the receiver. The SAR processor transforms the raw radar data into images which have to be analysed according to the relevant application. The system control data (orbit altitude and velocity, disturbances of the antenna trajectory etc.) are also used by the processor during the generation of SAR images.

Fig.2 shows a block diagram of the most important components of a SAR system. These components are basically used both for airborne as well as for onboard SAR systems. However, there are some differences concerning the processing of the raw radar data which can either take place onboard the carrying aircraft or in a ground station. In the latter case the radar data have to be transmitted by means of a telemetry system, as it will be done for ERS 1 and X-SAR.

The Real Time SAR Processor

The signal processing task of a real-time SAR processor is characterised both by complex algorithms to be implemented as well as by high input data rates. Even the most advanced computer systems are presently not able to solve this task by means of software programs.

Fig.3 shows the block diagram of a SAR processor. In a first step the demodulated radar signals are converted into digital information. Usually, real and imaginary I/Q data are used in the baseband for the representation of the amplitude and phase of the radar signal. Afterwards, the range compression of the raw data is performed. The linear range migration effect of the signal energy has to be compensated before the azimuth compression and look summation can take place. The "corner turn memory" converts the processing direction from range into azimuth. The azimuth processing is succeeded by the "post-processing". In this unit the processing is changed to range direction, again. Additionallly, the correct pixel mapping of the compressed radar data is done in this unit.

The "Doppler Estimator" and "FM Estimator" units derive the characteristics of the azimuth reference function either from the radar data itselves or from the orbit and attitude data of the antenna.

Concerning processing rate requirements in terms of millions of arithmetic operations per seconds (MOPS) under real time conditions, range and azimuth compression (see Fig. 3) are the most demanding units within the processor. Given the ERS 1 SAR parameters, roughly 900 MOPS are necessary for range compression in the frequency domain, whereas 350 MOPS must be performed for azimuth compression using the SPECAN algorithm.

Processor Implementation

A pipeline architecture as shown in Fig. 4 is most suitable for realtime digital SAR processing. The raw radar data enter the pipeline at the left hand side and are transformed - step by step - into the focussed image. This structure can be well compared to a manufacturing line in which the final product is assembled at different stations working at the same time on products which show different degrees of completeness.

The processing pipeline consists of digital hardware modules like Fourier transformation, interpolation, lowpass filter, twodimensional data memory, complex multiplication etc. the sequence and number of which are determined by the algorithm to be implemented by the processor. Several identical pipelines can be used in parallel if the requirements in terms of processing speed cannot be met by a single channel.

The processing parameters of each pipeline module are provided by the assigned pipeline controller. These controllers compute local module control parameters from some global control information which is received and distributed by the supervisor controller.

The processor hardware was implemented under the aspect that each specifically designed hardware module must include enough commonallity and flexibility to make it a part of a more general signal

processing hardware family. This concept allows the functional modules to be used at several places of the processor or even supports the implementation of different image processing tasks (e.g. other SAR algorithms, pattern recognition etc.) at very low development cost by using the same hardware modules in different arrangements.

All hardware modules incorporate identical electrical and mechanical interfaces in order to guarantee full modularity within the pipeline. Power saving CMOS technology has been chosen as far as possible to cover applications which suffer from lack of electrical energy (e.g. mobile processing in aircrafts etc.). 16 bit word length of both the real and imaginary data channel is offered by all modules allowing the hardware to handle the full dynamic range of present SAR systems.

Some features of the more important modules of the pipeline SAR processor are described in detail in the subsections below.

High speed storage unit:

Intermediate storage of data frames is a most important function of any kind of image processing. In a SAR processor these memories are used during corner turning, look summation, recorner turning and test pattern generation. In order to cover the above applications a universal memory board has been developed which allows for writing and reading line based data in both azimuth and range direction. The length of a line can be programmed within the limit of 256k words. The memory boards can easily be cascaded if more than 256k words of memory size is required for a specific application.

Dynamic NMOS memory chips and Advanced Low Power TTL control circuits are used for the board the mechanical size of which conforms to double eurocards. A read/write speed of up to 3 Mwords/sec could be achieved at a power consumption of 3.2 Watt only. Refresh circuits for the dynamic NMOS chips are included on the board.

A complete memory system (e.g. corner turn memory) for data frames of 1024 x 256 words is built up of three memory boards and a simple controller board which provides the correct input/output interface and some trigger signals, which tell the memory boards when to read or write data frames.

Finite impulse response (FIR) filter:

FIR filters are widely used for low pass filtering, bandpass filters in combination with a complex premultiplication, digital interpolation and correlation. In a SAR processor all functions mentioned above are required at different places of the pipeline.

A FIR filter offering programmable length of up to 256 samples has been developed using CMOS multiplier/accumulator circuits and CMOS/TTL control logic. The board is able to perform all functions des-

cribed above. In case of low pass filtering the output data can be subsampled by noninteger factors. The filter coefficients can be downloaded from the assigned pipeline controller. Up to 256 different filter sets can be stored at a time.

The maximum input data rate is given by the internal 20 MHz computation clock and the selected filter length.

Fast Fourier transformation (FFT) module:

A radix 2 decimation in time algorithm has been chosen for the high speed FFT module. This unit shows the following features:

- complex input/output 16 bit I / 16 bit Q
- programmable FFT length (2 up to 4096)
- FFT or inverse FFT selectable
- data weighting function loadable from external source
- programmable gain
- complex butterfly operating at 15 MHz
- full CMOS technology

A 4k FFT can be performed at a rate of 600 Hz whereas a shorter length of 32 runs at almost 140 kHz.

There is a wide range of applications for this module. Within the SAR processor both range and azimuth compression rely on this function in case of longer replica lenghts of the respective reference function. For shorter replica lengths also a time correlation solution might be selected as the proper hardware choice.

A prototype real time SAR processor for 1024 range samples of range compressed SAR data has been built on the basis of the pipeline architecture as described above. This processor is able to handle both ERS 1 and X-SAR data by simply initializing the processor according to the specific requirements of the actual SAR. The power consumption of the complete processor amounts to 120 watt thus demonstrating the efficiency of the hardware concept also in terms of electrical power requirements.

Further SAR Processor Activities

The developed SAR processor has proven the feasability of digital real-time SAR signal processing. An operational SAR processor including range compression and the Mean Doppler and FM Estimator units is presently being developed for the ground station of the X-SAR project.

A Quicklook processor for airborne SAR processing (DOSAR) is also being designed and developed within 1988. This processor will include additional functions for motion compensation.

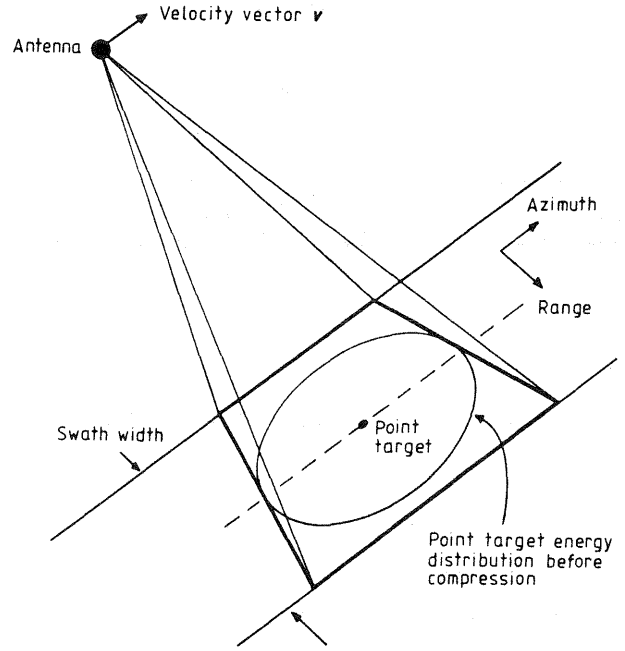

Fig. 1: Basic SAR Geometry

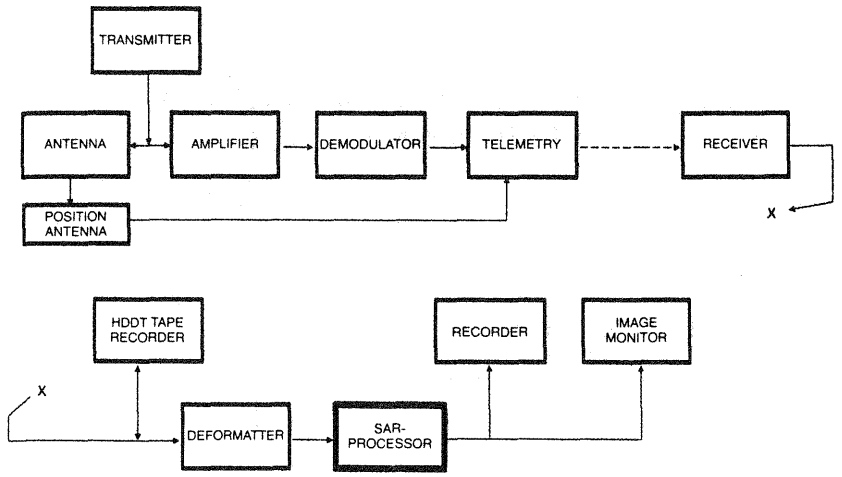

Fig. 2: Block Diagram of SAR System

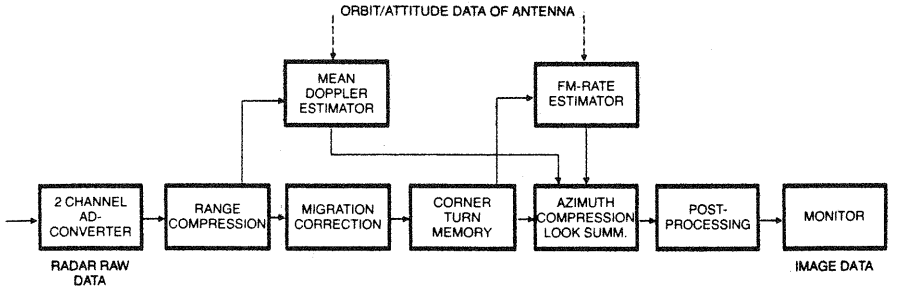

Fig. 3: SAR Processor Functions

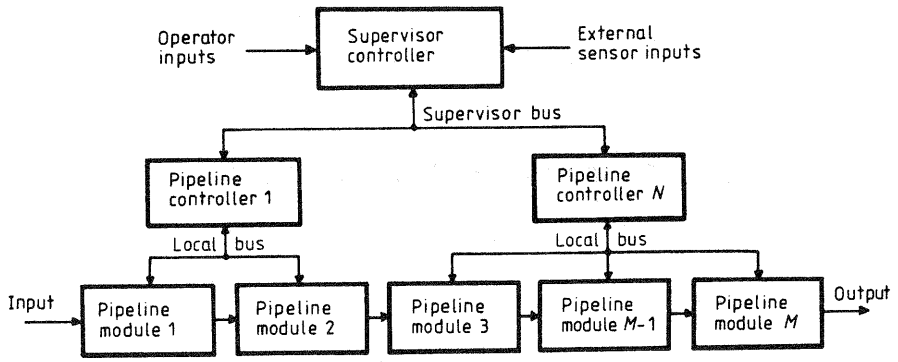

Fig 4: Block Diagram of Pipeline Architecture