DESIGN ASSESSMENT OF A HIGH PRECISION SAR PROCESSOR EMPLOYING THE TRANSPUTER BASED MEIKO COMPUTING SURFACE

J J W Wilson*
Centre for Parallel Computing
Queen Mary College
University of London
Mile End Road
London E1 4NS
England

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1. The T800 Transputer

The INMOS T800 transputer integrates a 32-bit CPU, a 64-bit floating point unit 4 Kbytes of RAM, four standard transputer communication links and peripherals and memory interfacing on a single chip fabricated in 1.5 micron CMOS technology. The transputer allows compact programmes and efficient implementation of high level languages, and, in addition it provides a medium in which to implement the Occam model of concurrency. The T800 achieves a sustained floating point performance in excess of 1.5 MFLOPS (at 32-bits) and 1.1 MFLOPS (at 64-bits) at 20 MHz. It employs a DMA block transfer mechanism to transfer messages from memory to other transputers via the standard transputer communication links. These links can transfer data at a sustained undirectional rate of 1.74 Mbytes s^{-1} or at a sustained bidirectional rate of 2.35 Mbytes s^{-1}. Data transfer via the links may be carrried out in parallel with processing. Each T800 transputer has 4 Kbytes of on-chip SRAM which may be accessed either by the links or by the processor. A 32-bit wide bus connects to external memory, thus extending the linear address space up to 4 Gbytes. The bus interface multiplexes data and address lines and supports a data rate of up to 4 bytes every 3 processor cycles thus giving 26.6 Mbytes s^{-1} for a T800 transputer driven at 20 MHz. A configurable memory controller provides all timing, control and DRAM refresh signals for a wide variety of mixed external memory systems.

2. The Meiko Computing Surface

The Meiko computing surface is a flexible, extendable multiprocessor computer system employing transputers. The flexibility contained in such an architecture arises from the freedom to choose both the number of transputers in the multiprocessor system and their topological connectivity. The elements from which a computing surface is constructed all have a basic common structure containing a transputer, a network interface, off-chip memory and a supervisor unit and a supervisor bus interface. In addition to the above, all but the basic computing element have additional specialised hardware units which perform a dedicated I/O functions. The following elements are now available: the Local Host, the Computing Element, the Mass Store, the Display Element, the Data Port

* **formerly of Marconi Research Centre**

Element and the Frame Grabber. At least one local Host Element is required in any Meiko Computing Surface to perform house-keeping tasks.

3. Algorithm Selection and Execution Timing

The SAR processor is required to produce a (99 km square) basic precision multilook SAR image, satisfying the European Space Agency's ERS-1 SAR image quality requirements, in 20 minutes.

Time domain SAR processing is extremely demanding in terms of computational load. Thus time domain SAR processing algorithms are never favoured over frequency domain SAR processing. algorithms on computer systems employing general purpose (non-dedicated) hardware. A precision frequency domain algorithm is therefore selected for implementation on the Meiko computing surface.

The selected algorithm in now described and its execution time calculated.

3.1. Range Processing

For range processing the raw SAR echo data range lines are processed on a line by line basis. The range processing of a single range line entails the following operations:

(A) Floating and Rescaling (32 IF statements)
5614 x 32 x 2.13 μs = 0.38266 s

(B) Forward Transformations
(4096 FFT + 2048 FFT + 1024 FFT)
336ms + 154ms + 69.2ms = 0.5592 s

(C) Range Compression Reference Function Multiplication
7168 x 5.38 μs = 0.03856 s

(D) Reverse Transformations
(4096IFFT + 2048IFFT + 1024IFFT)
336ms + 154ms + 69.2ms = 0.5592

E) Elevation Gain Correction Function Multiplication
4910 x 33.3 μs = 0.01635

One T800 transputer requires 1.556 s to execute the range processing of a single range line. The total number of range lines to be processed is 26784. Thus range processing takes 11 hours and 35 minutes on one T800 transputer. And therefore at least 34.73 T800 transputers will be required to execute range processing in 20 minutes.

3.2 Azimuth Processing

For Azimuth processing the range compressed SAR data is partitioned into overlapping azimuth blocks each comprising 80 azimuth lines of 1024 complex samples. After azimuth processing each such azimuth block yields 120 azimuth lines of image data, each comprising 410 samples. The azimuth processing of a single azimuth block entails the following operations:

(A) Forward Transformations
(80 x 1024 FFTs)
80 x 69.2 ms = 5.54 s

(B) Range Migration Correction Interpolations
(10 point interpolator acting on each of the 8 looks)
8 x 60 x 144 x 2 x 40.6 μs = 5.62 s

(C) Azimuth Compression Reference Function Multiplication
8 x 60 x 144 x 5.38 μs = 0.372 s

(D) Reverse Transformations
(8 x 60 x 512 FFTs)
8 x 60 x 31.2 ms = 14.98 s

(E) Pre-Detection Range Resampling
(10 point interpolator acting on each of the 8 looks)
8 x 120 x 410 x 2 x 40.6 μs = 31.97 s

(F) Detection
8 x 120 x 410 x 3.2 μs = 1.26 s

(G) Weighted Look Summation
120 x 410 x 29.02 μs = 1.43 s

(H) Fixing
120 x 410 x 2 μs = 0.1 s

One T800 transputer requires 61.28s to execute the azimuth processing of a single azimuth block. The total number of azimuth blocks to be processed is 3400. Thus azimuth processing takes 57 hours and 53 minutes on one T800 transputer. And therefore at least 173.63 T800 transputers will be required to execute azimuth processing in 20 minutes.

3.3 Processing Overheads

The processing power of a single computing element is reduced by overheads associated with data transfer through the element. In the worst case, this degredation is proportional to the amount of bandwidth to external memory which is used up by transfer transactions. It is necessary to compensate for this overhead by increasing the processing capability of the system; this increase is effected by the addition of further computing elements.

Assuming the raw data is packed as one real sample per byte, the raw data rate into the system is given by:
$(5614 \times 26784 \times (8+8))/(8 \times 1200) = 0.251$ Mbytes s^{-1}.

Assuming the range compressed data is packed as one real sample per 4 bytes, the range compressed data rate to Buffer Storage is given by:
$(80 \times 100 \times (32+32) \times 34816)/(8 \times 1200) = 1.857$ Mbytes s^{-1}.

Likewise the range compressed data rate from Buffer Storage is given by:
$(80 \times 1024 \times (32+32) \times 3400)/(8 \times 1200) = 1.857$ Mbytes s^{-1}.

Assuming the image data resulting from azimuth processing is packed at one sample per 2 bytes, the image data rate out of the system is given by:
$(8000 \times 8000 \times 16)/(8 \times 1200) = 0.107$ Mbytes s^{-1}.

The average data rate within the system may be taken to be half the data rate at the front end, thus we take:
$(0.251 + 1.857 + 1.857 + 0.107)/2 = 2.04$ Mbytes s^{-1}.

The amount of bandwidth to external memory used up by this data transfer within a single transputer is (with reference to Figure 1) given by:
(2.04 x 2/32) = 0.128 Mbytes s^{-1}.

The total bandwidth to external memory within a single computing element is of the order of 20 Mbytes s^{-1}. Thus the overhead is given by:
(0.128/20) = 0.7%

On the basis of the number of transputers required for range and azimuth processing and the calculated percentage allowance for data transfer overheads, we may now compute the total number of T800 transputers required.

Range Processing	34.73
Azimuth Processing	173.63 +
	208.36
Data Transfer O/H	1.46 +
	209.82

Therefore 210 T800 transputers will be required by the multiprocessor system for SAR processing operations.

4. Architectural Configuration and Operation

The architecture of the SAR processor is shown in Figure 1. Data enters the system via a host computer which carries out both auxiliary processing and data unpacking operations. The host computer provides the external interface to the SAR processor. Input data passes into the computing surface through the Data Port bus which interfaces to the host computer bus. The interface hardware between the host computer bus and the Data Port bus resides within the computing surface. The Data Port bus supports data rates of up to 80 Mbytes s^{-1}. Eight Data Port Elements are attached to the Data Port bus; this provides 32 standard transputer communication links into the computing surface.

The computing surface consists of a modified butterfly network which permits high data flow in both dimensions of the plane of the computing surface. The butterfly network consists of 192 (=32 x 6) Computing Elements. The modifications to the butterfly network are the following: Firstly, the 32 Computing Elements in the butterfly structure closest to the Data Port bus are attached to 32 additional computing elements with increased memory which act as buffer storage for azimuth block assembly between range and azimuth processing. Secondly, the 32 computing elements in the butterfly network farthest from the Data Port bus are attached to 18 additional Computing Elements which are required to increase the number of transputers in the system, using for processing, to the required level of 210 (=192+18).

Each raw SAR echo data range line is fed into the computing surface and transmitted to a free Computing Element where it is subjected to range processing. The resulting range compressed data is divided into overlapping segments corresponding to the individual range line segments in an azimuth block. The range compressed range line segments from the entire computing surface are transmitted to pre-determined buffer storage where they are assembled into azimuth blocks. When an azimuth block has been assembled it is transferred from buffer storage to a free Computing Element where it is subjected to azimuth processing. After azimuth processing, the resulting image data block is transferred out of the computing surface via the host computer for assembly on disk storage.

Each Computing Element has 1 Mword of memory except for the 32 Buffer Storage Computing Elements which have 4 Mwords of memory. This allocation should be sufficient for both data and code storage.

5. Equipment Requirements

The following hardware would be required to construct the system (described in section 4):

(1) 210 T800 Computing Elements each with 1 Mword of storage (53 Boards)
(2) 32 T800 Computing Elements each with 4 Mwords of storage (16 Boards)
(3) 8 T800 Data Port Elements (4 Boards)
(4) 1 Host Computer Bus/Data Port Bus Interface Unit (2 Boards estimated)
(5) 3 Intercabinet Interconnect Units each with 16 links (3 Boards)
(6) 2 Local Host Elements (2 Boards)
(7) 2 M40 Equipment Shroud Units in which to accommodate the above boards

6. References

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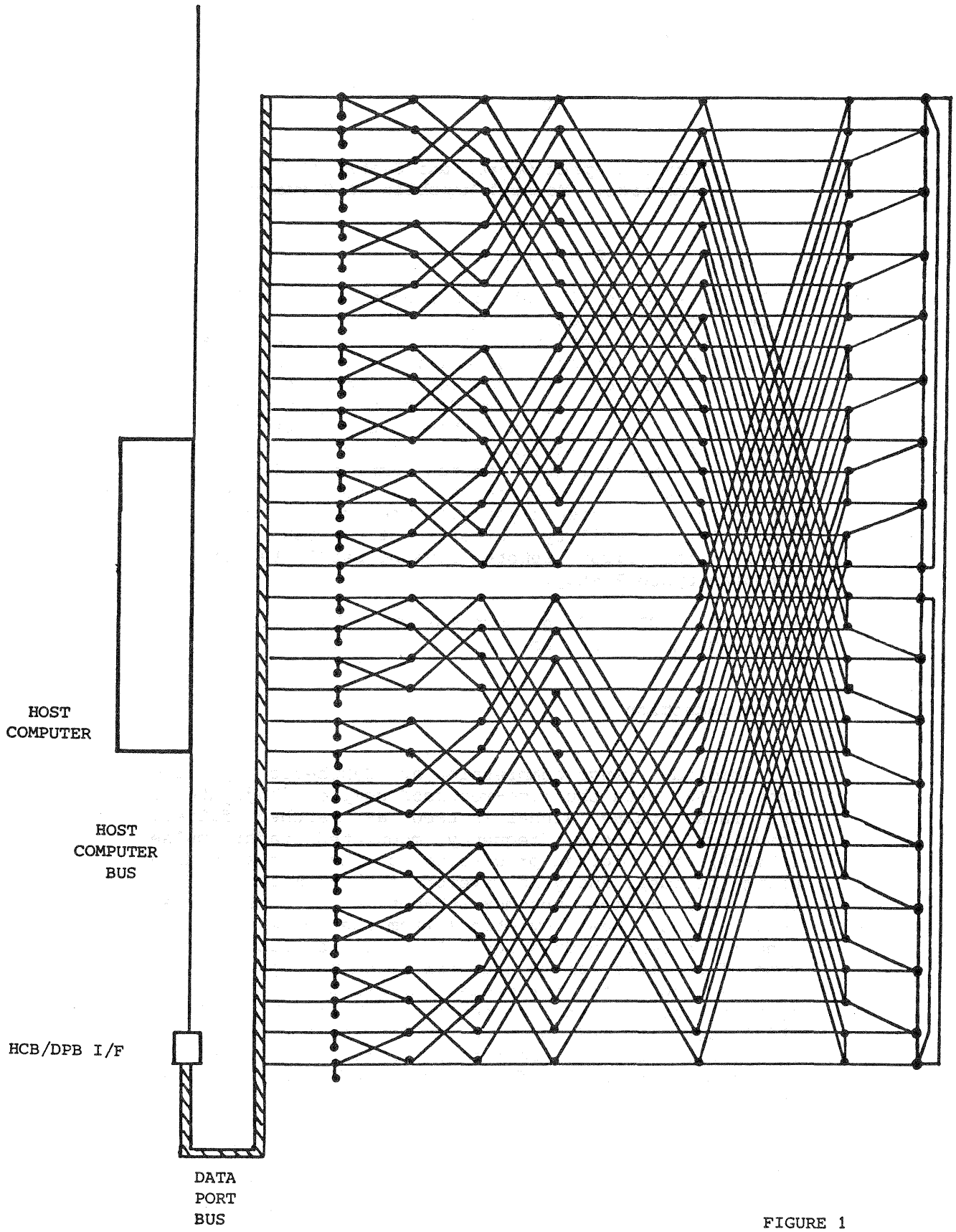

FIGURE 1